TOTAL IONIZING DOSE RADIATION EFFECTS AND NEGATIVE BIAS TEMPERATURE INSTABILITY ON SiGe *p*MOS DEVICES

By

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Thesis

Submitted to the Faculty of the

Graduate school of Vanderbilt University

in partial fulfillment of the requirements

For the degree of

MASTER OF SCIENCE

in

Electrical Engineering

May, 2014

Nashville, Tennessee

Approved by:

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ACKNOWLEDGEMENTS

First, I must offer truly heartfelt thanks to my advisor Prof. Daniel M. Fleetwood. It would be impossible to achieve my Master's degree without his help. It has always been a great pleasure for me working under his guidance for my Master's degree. He has always offered me professional guidance and shown me different ways to solve research problems. His profound knowledge and religious research attitude inspire me not only in the research but also in my life. I am lucky to have him as my advisor. I would also like to thank Prof. Ronald D. Schrimpf for sharing his knowledge through countless discussions when I encounter difficulties in research every Monday morning.

Many other people contributed to this work. I would like to especially thank Dr. Enxia Zhang. She has been teaching me how to use the experimental equipment and how to package the devices. Without her help, I would not perform my experiment. Then I would like to thank Jin Chen who provided me some MATLAB codes, Jordan Hachtel who helped me get STEM pictures of devices used in this work, and collaborators from imec and SEMATECH. I would also like to thank the Air Force Research Laboratory for funding for this research.

Finally a big thank you goes to Dr. Cher Xuan Zhang for providing support for my work and in life.

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CHAPTER I

INTRODUCTION

For the past four decades, the performance of Metal-Oxide-Semiconductor (MOS) transistors has increased tremendously due to continuous and aggressive downscaling of MOS devices. In order to obtain a constant electric field to keep the transistor properly function, all the voltages and dimensions are downsized by an equal factor. Gate oxide thicknesses have been scaled from nanoscale (~100 nm) to atomic scale (~1 nm). The minimum thickness for ideal bulk SiO_2 oxide is about 0.7 nm [1], which is only two atomic layer of silicon oxide. Considering the interface roughness, a lower limit of 1.2 nm is put on the practical SiO_2 gate oxide thickness [2]. One of the major challenges for further down-sizing the scale has been searching for ultrathin gate dielectric materials. Replacing the ultrathin SiO_2 with physically thicker high-k materials has helped to overcome the physical constrains and gate leakage current issues.

Not every high-k oxide can be a good substitute for SiO_2. Thermal Si oxide, which has been studied intensively for more than 40 years, forms an excellent interface with the Si. In addition to the high dielectric constant compared to SiO_2, there are several requirements for high-k materials that can be used as a MOS gate dielectric material. They must be thermodynamically stable with the Si channel and the gate electrode, and they should be kinetically stable and be compatible with processing to no less than 500 ℃. Moreover, they should have band offsets with Si of over 1 eV so that the carrier injection into the oxide is minimized, good interface with Si, and low bulk oxide trap density. Table 1 summarizes various

characteristics and main features of several alternative high-k gate dielectrics that were considered as potential materials for MOS gate dielectric applications.

Table 1. Comparison of the major characteristics, advantages, and disadvantages of existing and potential high-k gate dielectrics (After [1]).

Dielectric	Dielectric constant	Bandgap (eV)	Conduction band offset (eV)	Merits	Drawbacks
SiO_2	3.9	8.9	3.15	Excellent Si interface, low Q_{ox} and D_{it}	Low-k
Si_3N_4	7-7.8	5.3	2.1	Good interface and bulk properties, medium Q_{ox} and D_{it}	Low-k
Al_2O_3	9-10	8.8	2.8	E_g comparable to SiO_2, amorphous	Medium Q_{ox} and D_{it}, medium k
Ta_2O_5	25	4.4	0.36	High-k	Unacceptable ΔE_C, not stable on Si
La_2O_3	~27	5.8	2.3	High-k, better thermal stability	Moisture absorption, unstable with Si
Y_2O_3	~15	6	2.3	Large E_g	Low crystallization temperature, high D_{it}, silicide formation
HfO_2	~20	5.6-5.7	1.3-1.5	Most suitable compared to other candidates	Crystallization, silicate and silicide formation
ZrO_2	~23	4.5-5.7	0.8-1.4	Similar to HfO_2	High Q_{ox} and D_{it}, Marginal stable with Si, crystallization, silicide formation

High-k dielectrics have significantly reduced band gap and band offsets as compared to SiO_2, resulting in an increase of the gate leakage current via electron tunneling from channel to gate oxide. Moreover, an interfacial layer (SiO_x) usually forms between the high-k dielectric layer and the Si channel layer during metal oxide deposition [3], thus creating an additional contribution to equivalent oxide thickness (EOT),

$$\text{EOT} = \frac{\varepsilon_{high-k}}{\varepsilon_{SiO_2}} d_{high-k} + d_{SiO_2}$$

where ε_{SiO_2} and ε_{high-k} are the dielectric constant of silicon oxide and high-k material, respectively. d_{SiO_2} and d_{high-k} are the physical thickness of interfacial SiO_2 and high-k dielectric, respectively.

Si/SiO_2 interfaces can be made with a high quality, and the defects can be passivated by hydrogen. The presence of a SiO_2 layer that is compatible with the Si substrate can separate the high-k oxide from the Si channel, which reduces the remote scattering caused by the defects in high-k oxide.

Hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) have been demonstrated to be the most promising candidates to replace SiO_2 in MOS devices. They have shown similar promise in overall materials properties. They have relatively high dielectric constants compared to Si_3N_4, Al_2O_3, and Y_2O_3, and better band offsets than most other high-k dielectrics, as shown in Fig. 1.1. The thermodynamic stability of the high-k dielectrics ZrO_2 and HfO_2 in contact with Si and SiO_2 has been calculated by Gutowski et al. [4]. The HfO_2/Si interface is found to be stable with respect to formation of silicides, whereas the ZrO_2/Si interface is unstable. The stable interface with silicon makes HfO_2 a preferred candidate to replace SiO_2 as a gate dielectric over ZrO_2.

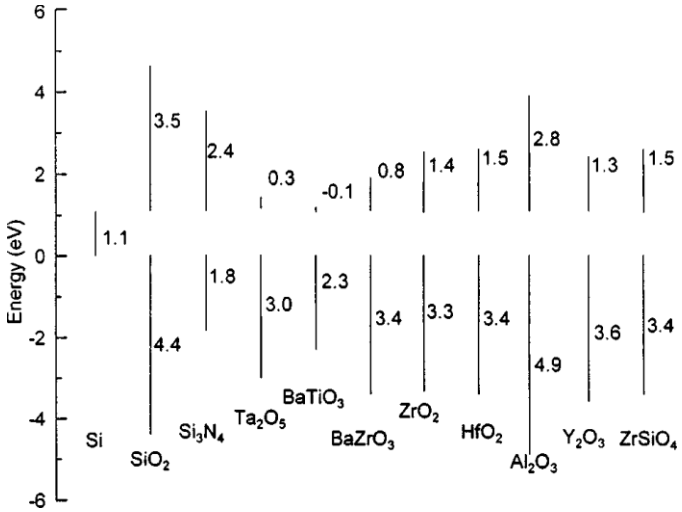


Fig. 1.1. Calculated conduction band and valence band offsets of various alternate oxides on Si. After [3].

In addition to the introduction of high-k material in MOS devices, the incorporation of several new material and structural changes probably will be required for continuing MOSFET evolution. People have been searching for alternative channel materials to replace silicon at the wafer surface, in an effort to improve the performance of MOS devices. Due to the high hole mobility and compatibility with standard silicon processes, silicon germanium (SiGe) is of great interest as an alternative channel material to achieve a performance boost of *p*MOSFETs [5]. Since the first SiGe *p*-channel FETs were demonstrated [6-7], MOS structures with SiGe channels have been receiving increasing attention. However, there are many issues that need to be solved for SiGe MOS devices. One of the significant issues concerning SiGe MOS fabrication is forming a stable interface between the gate dielectric and SiGe channel. Conventionally, a thin Si cap layer is used for SiGe surface passivation. The holes traveling in the SiGe channel are expected to have enhanced mobility by fundamentally altering the band structure of the channel due to the presence of the germanium. Furthermore, since the SiGe is separated from the gate oxide by a thin silicon cap layer, the surface scattering should be negligible.

It is necessary to evaluate the charge trapping characteristics and long-term reliability of SiGe/high-k structure devices for potential space-exploration applications. In this thesis, radiation response and bias-temperature effects on SiGe/high-k structure are explored. Chapter II reviews the basic total-dose effects and negative bias temperature stability (NBTI) in MOS systems. Chapter III focuses on the irradiation biases dependence of SiGe *p*MOS FinFETs as a function of total dose irradiation, and chapter IV describes the negative bias temperature stress results on SiGe-*p*MOSFETs. Chapter V summarizes and concludes the work.

CHAPTER II

TOTAL IONIZING DOSE AND NEGATIVE BIAS TEMPERATURE INSTABILTIY IN MOS DEVICES

The first part of this chapter contains background information about total ionizing dose effects in MOS devices. The midgap and subthreshold swing methods that are used in his work to separate the threshold voltage shifts due to oxide-trap charge (ΔV_{ot}) and interface-trap charge (ΔV_{it}) are described in detail. The second part of this chapter describes the mechanisms of negative bias temperature instability (NBTI) in MOS devices.

1. Total ionizing dose effects in MOS devices

The microelectronic components in space are exposed to various types of radiation such as protons and electrons, which interact with the semiconductor material to cause ionizing damage, atomic displacement, and/or single event effects. Total-dose irradiation is a significant concern for the long-term reliability of MOS devices. It is extremely important to understand radiation effects on semiconductor devices for the application of advanced technologies and materials in space environments. This section will discuss the basic effects of radiation-induced charge buildup in MOS devices, including oxide, interface, and border traps.

1.1 Basic mechanisms of total ionizing dose irradiation

Fig. 2.1 shows a schematic energy diagram of a MOS structure under positive bias applied to the gate and indicates four major physical processes that contribute to the radiation response of a MOS device. For MOS devices, the most total-dose radiation-sensitive parts are the

oxide insulators. When a MOS device is exposed to high-energy ionizing radiation, electron-hole pairs are created in the oxide by the deposited energy (process 1). Because the electrons are much more mobile (20 cm^2/V sec at 300 K in fused quartz [8]) than the holes (~4×10^{-9} cm^2/V sec at 300 K) in SiO_2, most of the electrons are rapidly swept out of the oxide (within picoseconds), and holes are trapped in micro-structural defects and pre-existing traps. However, even before the electrons leave the oxide, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the charge yield. The fraction depends greatly on the strength of the electric field in the oxide and the energy of the incident particle. The generation and recombination of electron-hole pairs are the first processes shown in Fig 2.1. Those holes that escape initial recombination will further transport toward the Si/SiO_2 interface by hopping via localized states in the oxide (process 2) [9]. This process typically takes less than a second [10], but may take place over many decades in time. Because hole transport in SiO_2 is highly dispersive [11], as a result, the "tail" of the transport extends over several decades in time.

As the holes approach the Si/SiO_2 interface, some fraction of the holes will be neutralized by electrons tunneling from silicon or thermal emission from the trap sites, and others will become trapped at relatively deep trap states, forming positive oxide trap charges (process 3). These oxide trapped charges can cause a shift in the threshold voltage and an increase of radiation-induced leakage current (RILC) in these devices. RILC involve an inelastic tunneling process assisted by neutral traps in the oxide. The neutral electron trap likely originates as radiation-induced holes trapped at E' centers (E' centers will be described in details later) in the oxide. The Electron Spin Resonance (ESR) measurements performed by P. M. Lenahan et al. have shown a link between E' centers and RILC [13].

Meanwhile, hydrogen ions (protons) can be released in the oxide bulk as holes transport toward the interface through the oxide. Those protons can drift to the Si/SiO_2 interface under positive gate bias where they may react with Si-H to form H_2, leaving silicon dangling bonds at the interface (process 4). These dangling bonds can act as interface traps, which are localized states in the Si band-gap. Their occupancy is determined by the Fermi level, leading to a change of threshold voltage and a decrease of carrier mobility.

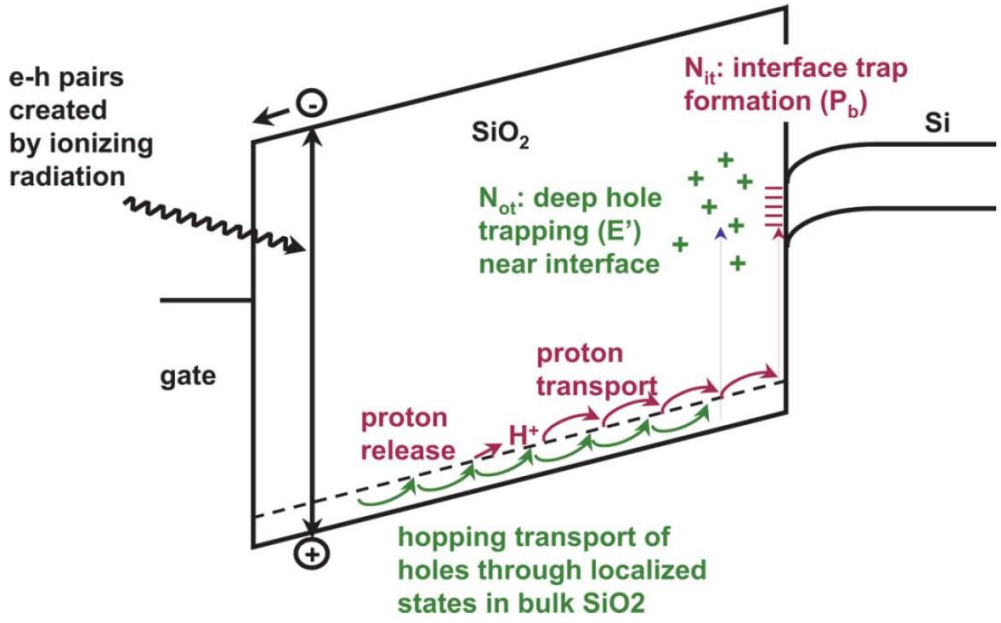


Fig. 2.1. Schematic energy band diagram for MOS structure under positive bias, indicating major physical processes underlying radiation response. After [12].

1.2 Charge yield

As previously mentioned, some fraction of the radiation-induced holes will recombine with the electrons before the electrons are swept out of silicon dioxide, in a time on the order of a picosecond. The fraction of holes escaping initial recombination (f_y) depends strongly on the magnitude of the electric field through the oxide. When an electric field is applied across the oxide of a MOS device, the radiation-induced electron-hole pairs will immediately be separated

and begin to transport in opposite directions. As the electric field strength increases to separate pairs more efficiently, the probability that a hole will recombine with an electron decreases, and the charge yield increases. Fig. 2.2 plots the fraction of holes that escape recombination for 10-keV x-ray irradiation as a function of the electric field. When the electric field is higher than 4 MV/cm, more than 80% of radiation-induced holes escape initial recombination.

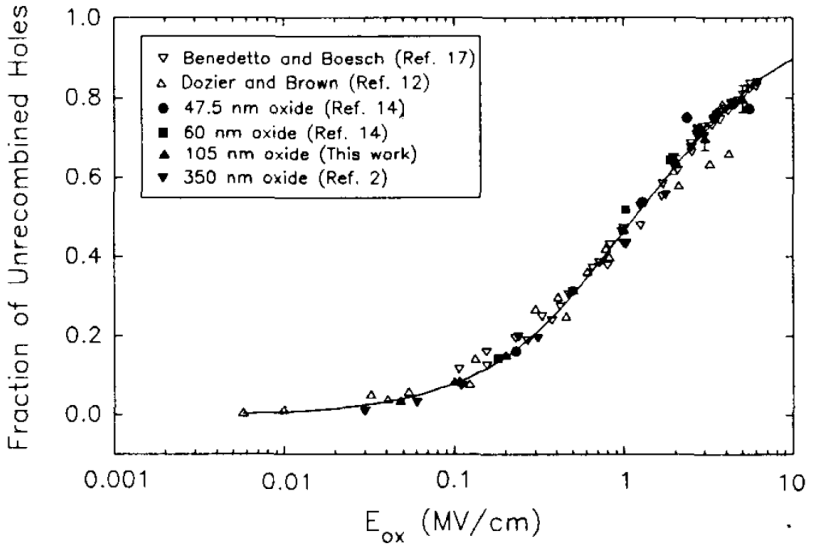


Fig. 2.2. Fraction of holes which escape rwombination for 10-keV x-ray irradiations as a function of oxide field. The solid line is a fit to data. After [14].

1.3 Defect types

In insulators, five general classes of defects have been recognized: fixed oxide charge, mobile ionic charge, interface-trapped charge, oxide-trapped charge [15], and border traps [16]. “Fixed oxide traps” and “oxide-trapped charge” are located within the oxide, and are not in electrical communication with the underlying Si. “Interface traps” are located at the Si/SiO_2 interface and in electrical communication with the underlying Si. Border traps are near-interfacial oxide traps that exchange charge with the underlying Si on the time scale of the measurements [16].

Oxide traps:

There are a large number of oxygen vacancies close to the interface where oxidation is not complete. The oxygen vacancy can be activated into the paramagnetic state by irradiation. That radiation-induced paramagnetic center is termed an E’ defect, which is identified as a "trivalent silicon” back-bonded to three oxygen atoms in the oxide. There is one oxygen atom missing from the usual Si-O-Si lattice configuration, leaving a weak Si–Si bond. That an E’ center is an oxygen vacancy can be verified by ESR. The relationship between E’ centers and radiation-induced trapped holes was first established by Lenahan and Dressendorfer [17]. Their experimental results indicated that the concentration of radiation-induced E' centers is approximately equal to the concentration of holes trapped in the SiO_2, that the distribution of E' centers and trapped holes in the oxide are similar, and that annealing characteristics of E’ centers and trapped holes are also similar. Therefore, E’ centers or oxygen vacancies are primarily responsible for hole traps in the thermal oxides of MOS devices.

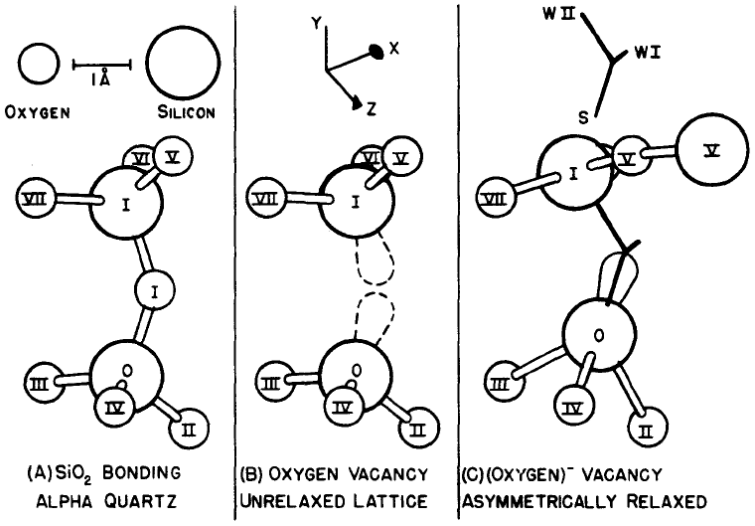


Fig. 2.3. Oxygen vacancy model for the E’ center in SiO_2. (a) Normal oxygen vacancy. An important feature is the existence of two inequivalent Si-O bonds. (b) Unrelaxed lattice oxygen vacancy. (c) Asymmetrically relaxed O^- vacancy.

F. J. Feigl, W. B. Fowler and K. L. Yip proposed an oxygen vacancy model (Feigl-Fowler-Yip model) for the E' center [18]. As illustrated in Fig. 2.3, after the hole is trapped in the precursor bridging-oxygen vacancy, a weak strained Si-Si bond configuration is broken. One of the Si atoms then relaxes back into a planar configuration, leaving it positively charged. The other Si remains neutral, with a dangling orbital containing one unpaired electron. An E' center consists of these two trivalent Si atoms together. The E' signal in ESR is actually obtained by resonant flipping of the spin of the unpaired electron on the neutral Si atom.

Interface traps:

In addition to oxide traps, radiation can also cause the formation of interface traps at the Si/SiO_2 interface. ESR studies by Lenahan et al. [19] showed a strong correlation between the buildup of radiation-induced interface traps and the buildup of the P_{b0} resonance. This P_{b0} center is also a "trivalent silicon", but in this case the silicon is bonded to three Si atoms, with a dangling bond extending into the oxide, as schematically represented in Figure 2.4 (that P_{b1} is designated as $Si_2O{\equiv}Si\bullet$ is not correct, and will be shown later). Because of the energy level within the Si bandgap and location at the interface, the interface defect is amphoteric, negatively charged above midgap, approximately neutral near midgap, and positively charged below midgap.

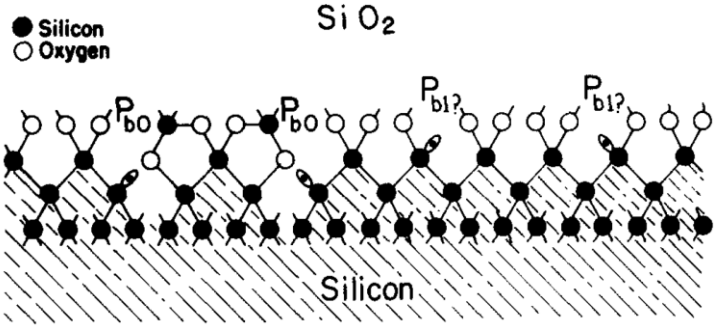


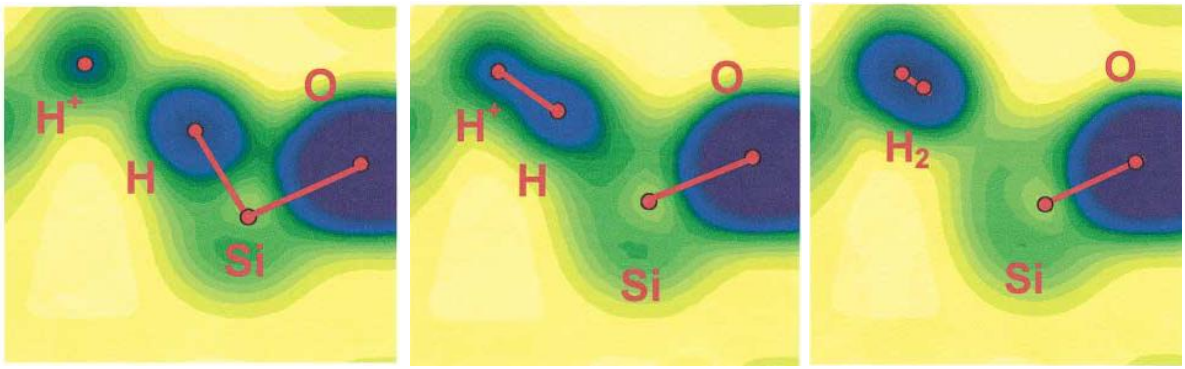
Fig. 2.4. Schematic representing the structure of a P_{b0} defect center at SiO_2/Si (100) interface. After [20].

The most widely accepted model for interface trap formation was described as a two-stage process involving hopping transport of protons by McLean [21]. In the first stage of this process, radiation-induced holes transport through the oxide, and release hydrogen ions (protons) in the SiO_2 bulk. In the second stage, the protons undergo dispersive hopping transport to the interface, react and break the Si-H bonds already there, forming H_2 and a trivalent Si defect (P_{b0} center).

Density functional theory calculations by Rashkeev et al. [22] strongly suggest that protons interact directly at the Si/SiO_2 interface via the simple reaction:

$$H^+ + Si\text{-}H = Si^+ + H_2$$

Fig. 2.5 traces the computed electric density contours in the region around a Si dangling bond passivated by hydrogen at the Si/SiO_2 interface during the depassivation process. The calculations suggest that two electrons leave the Si-H through $Si\text{-}H\text{-}H^+$ bridge, forming a neutral H_2 molecule and leaving a dangling bond positively charged.



(a) (b) (c)

Fig. 2.5. Electronic density at different stages of the reaction between H^+ and a Si-H bond: (a) a proton approaches a Si-H bond; (b) an $Si\text{-}H\text{-}H^+$ bridge is created; (c) an H_2 molecule and a D^+ defect are formed. After [22].

Border traps:

A standard name for near-interfacial oxide traps that communicate with the Si was proposed as "border traps" by D. M. Fleetwood in 1992 [16]. Border traps are defined as near-interfacial oxide traps that are able to rapidly or slowly exchange charge with the underlying Si substrate over a very wide range of time scales. There is growing evidence that a large percentage of these defects are likely associated with E' centers [16,23,24]. Border traps typically are located within a certain distance (~2 nm) in the oxide from the interface, as shown in Fig. 2.6.

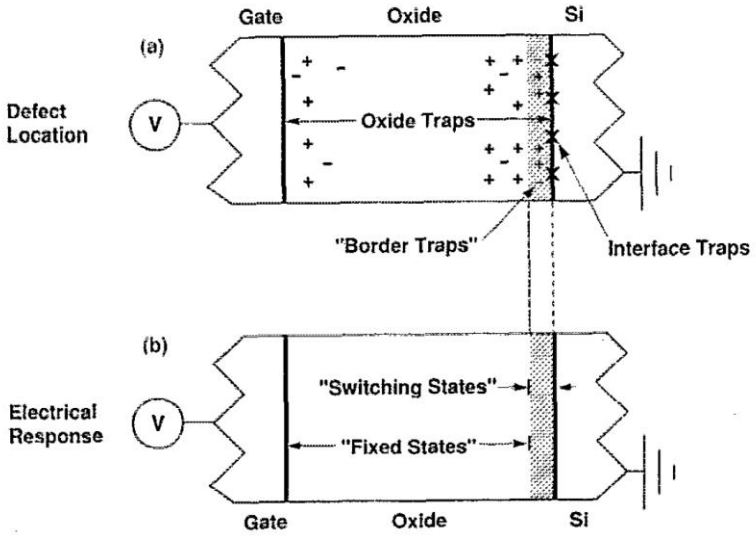


Fig. 2.6. Schematic representation of (a) the physical location of oxide, interface, and border traps and (b) their electrical response. After [25].

1.4 Charge separation techniques

To separate the effects of oxide and interface trap charge, the overall radiation response of a MOS device needs to be separated into its components:

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \quad (1)$$

Here ΔV_{ot} and ΔV_{it} are the threshold voltage shifts due to oxide traps and interface traps, respectively. There are different methods for separating ΔV_{th} into its components.

Midgap charge separation method:

The midgap charge separation method is based on the observation that the interface traps are approximately charge neutral for a device biased at midgap [26],[27]. The interface traps are amphoteric. In the upper portion of the band gap the interface traps are mostly acceptor-like. These are negatively charged when filled and neutral when empty. In the bottom portion of the band gap they are donor-like; these are neutral when filled and positively charged when empty. In this case, the radiation-induced net oxide-trapped charge density can be estimated by the shifts in the midgap voltages (ΔV_{mg}) before and after irradiation:

$$\Delta V_{ot} = \Delta V_{mg} \tag{2}$$

$$\Delta V_{it} = \Delta V_{th} - \Delta V_{mg} \tag{3}$$

The midgap voltages (V_{mg}) can be determined from subthreshold-current curves, as illustrated in Fig. 2.7.

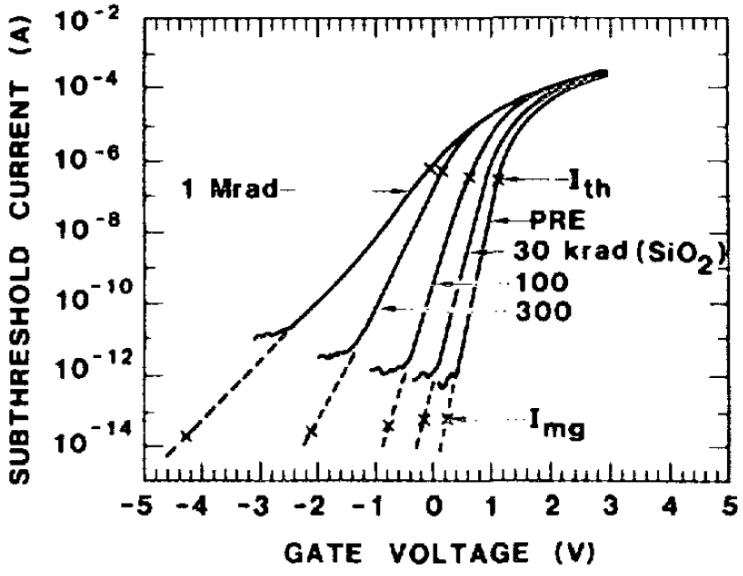


Fig. 2.7. Subthreshold-current curves for an MOS transistor before and after irradiation. After [26].

The radiation-induced interface trap charge density (ΔN_{it}) and oxide trap charge density projected to the Si/SiO_2 interface (ΔN_{ot}) were estimated for MOS capacitors by the following equations:

$$\Delta N_{ot} = -C_{ox}\frac{\Delta V_{mg}}{qA} \tag{4}$$

$$\Delta N_{it} = C_{ox}\frac{(\Delta V_{th} - \Delta V_{mg})}{qA} \tag{5}$$

Here C_{ox} is the oxide capacitance, –q is the electronic charge, and A is the area.

Subthreshold swing method:

The subthreshold technique is based on standard I-V characteristics [27]. When plotted as log I_D versus V_G, comparing the pre- and post-irradiation characteristics, the change in subthreshold swing, ΔS, can be determined. The subthreshold swing method of the charge separation technique is based on the calculation of the radiation induced voltage shift due to interface traps, ΔV_{it}, using the change subthreshold swing, ΔS:

$$\Delta V_{it} = \frac{q\phi_s}{kT\ln 10}\Delta S\,, \tag{6}$$

$$\Delta V_{ot} = \Delta V_{th} - \Delta V_{it}\,, \tag{7}$$

Here ϕ_s is the surface potential, k is Boltzmann's constant, and T is the absolute temperature.

2. Negative bias temperature instability

Among the various reliability issues in modern CMOS technology, negative bias temperature instability (NBTI) has become one of the most serious concerns for highly scaled *p*MOSFETs. NBTI is associated with the creation of oxide and interface trap charge at the Si/oxide interface, when negative bias is applied to the gate at elevated temperatures. NBTI has a

significant impact on *p*MOSFETs since those devices work under negative bias condition during high-performance chip operation. Although NBTI has been known for more than 30 years, the mechanism for NBTI is still under debate. NBTI has often been interpreted by some form of reaction-diffusion model originally proposed by Jeppson and Svensson [29]. The RD model is diffusion controlled and assumes that Si-H bonds at the semiconductor/oxide interface are broken at higher temperatures and electric fields, causing some hydrogen species released from previously passivated interface defects and then dispersively diffuse into the oxide [30].

Another NBTI model in form of RD model proposed by L. Tsetseris et al. [31] involves the depassivation of dopants in Si and subsequent movement of hydrogen species to the interface. First-principles calculations show that a direct depassivation reaction, $Si_3{\equiv}SiH + H^+ \rightarrow Si_3{\equiv}Si\bullet + H_2$, is in fact possible. Here $Si_3{\equiv}SiH$ is a hydrogen-passivated interface trap and $Si_3{\equiv}Si\bullet$ an interface trap with the dot representing the dangling bond. The hydrogen is assumed to be released from P-H bonds as the n-type Si surface is biased to depletion at elevated temperature. The hydrogen becomes positively charged (H^+) by trapping a hole. H^+ is swept to the interface by the negative bias, and subsequently reacts with the Si-H bond to form H_2 leaving behind a positively charged Si dangling bond (or P_b center). The H_2 diffuses from the interface into the oxide.

However, recent studies of NBTI [32-33] find that interface-trap creation is not the sole source of degradation but a major hole trapping effect also occurs. Additionally, a large number of detailed recovery studies published in the last decade [33-34] cannot be fully accounted for by the reaction-diffusion mechanism family. As a consequence, recent research focus has shifted back toward charge trapping. Interestingly, this hole trapping mechanism was was also suggested in the pioneering paper on the RD model by Jeppson and Svensson [29].

In 2009 Grasser et al. proposed a two-stage model able to capture a large number of the features [35], suggesting the degradation is due to interface trap generation and/or oxide charge buildup. The degradation is assumed to proceed in two coupled stages. For the first stage, the NBTI degradation process is initiated (stage 1) when inversion layer hole capture occurs at E' precursor sites, e.g., a neutral oxygen vacancy. The hole capture leads to positively charged E' centers (paramagnetic defects observable with ESR) in the oxide, thereby creating a switching trap, as illustrated in Fig. 2.8. Initially, a neutral precursor exists (state 1). Upon hole capture, the Si–Si bond breaks and a positively charged E'_{γ} center is created (state 2). Hole emission (electron capture) neutralizes the E'_{γ} center (state 3). Being in state 3, two options exist: a hole can be captured again, causing a transition to state 2, or the structure can relax back to its equilibrium configuration (state 1). For the second stage, oxide silicon dangling bonds (E' centers) created in the stage one process trigger the creation of P_b centers via hydrogen exchange with a P_b center at the interface.

J. P. Campbell et al. [36] utilized spin-dependent recombination (SDR) to observe and identify atomic-scale defect centers generated by a negative bias temperature in *p*MOSFETs. In SiO_2 devices, the defects include two silicon dangling bond centers (e.g., P_{b0} and P_{b1} defects schematically shown in Fig 2.9) at the Si/SiO_2 interface and may also include oxide silicon dangling bond center (E'). J. T. Ryan et al. [37] performed ESR measurements that further confirm that positively charged oxygen vacancy sites (E' centers) are generated during NBTI stress and very quickly recover upon removal of the stress. The E' defect density does not change during zero oxide bias at elevated temperature or negative oxide bias at room temperature. These observations support hole capture at an E' precursor site and the depassivation of interface traps.

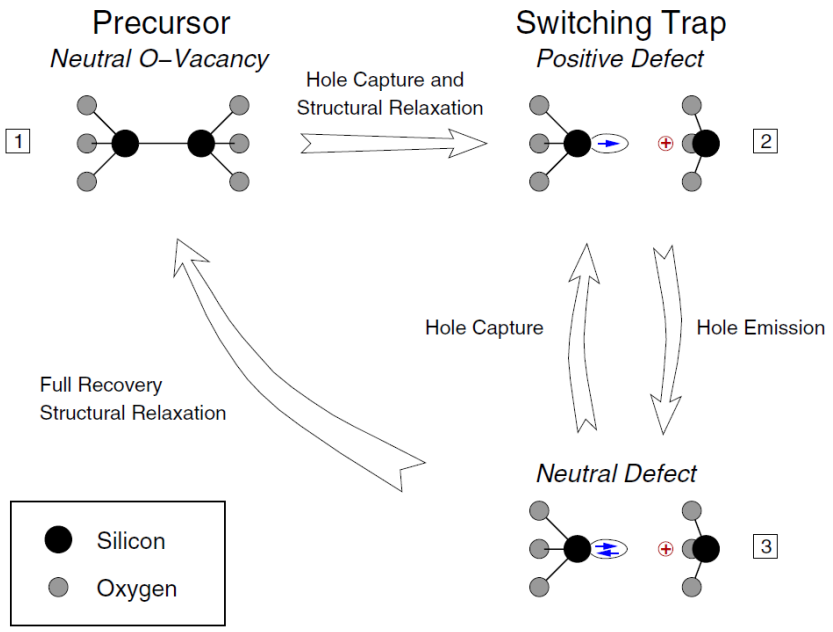


Fig. 2.8. Switching oxide trap model. After [35].

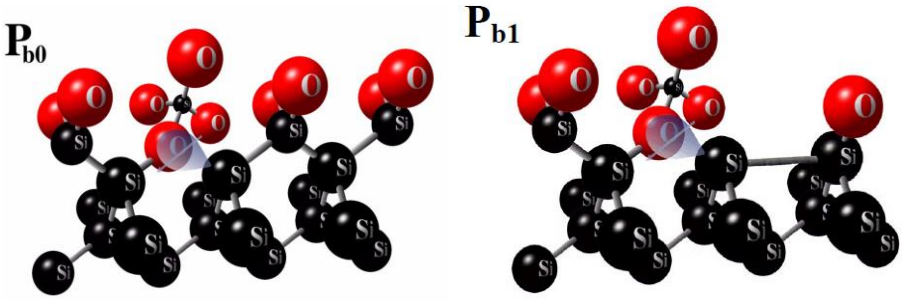


Fig. 2.9. Schematic diagrams of P_{b0} and P_{b1} Si/SiO_2 interface traps. After [37].

Although all models have been in controversy, the mechanism is ascribed to two kinds of traps: one is associated with breaking of Si-H bonds at the SiO_2/Si interface by a combination of electric field and elevated temperature, resulting in dangling bonds (P_b center) at that interface; the other is associated with positive oxide trap (E' center), which may be due to H^+ or trapped holes.

CHAPTER III

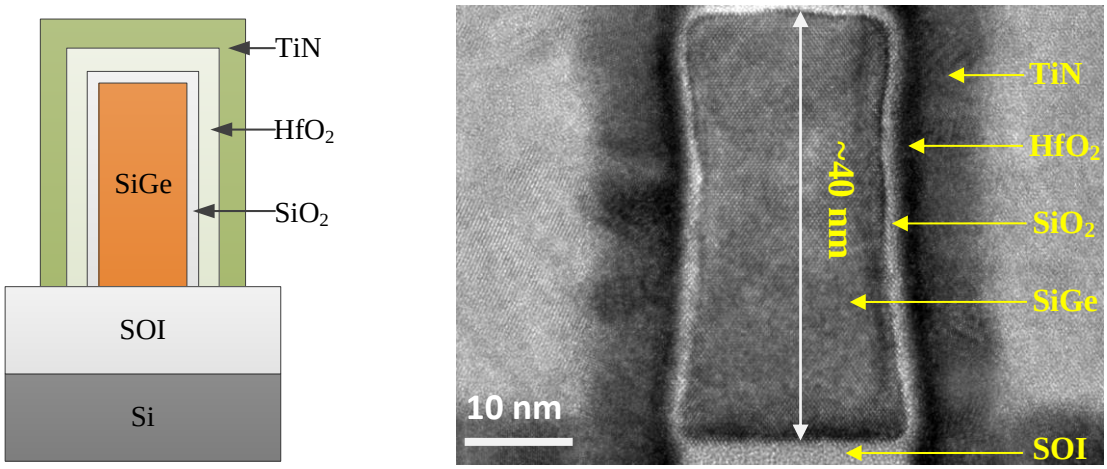
TOTAL-DOSE EFFECTS IN SILICON GERMANIUM *p*MOS FINFETS

This chapter explores the effects of 10-keV X-ray irradiation on SiGe *p*MOS FinFETs with a SiO_2/HfO_2/TiN gate stack. Hafnium oxide (HfO_2) is increasingly replacing SiO_2 as a MOS gate dielectric in highly scaled devices due to its high dielectric constant, relatively large band gap and high thermal stability [38],[39]. Strained SiGe has attracted great attention as a promising alternative channel candidate material to boost *p*MOSFET performance for sub-22 nm technologies because of its enhanced hole mobility [40]. High performance *p*MOSFETs that combine SiGe channels and HfO_2 gate dielectrics are therefore promising candidates for next generation CMOS ICs [41]. These devices usually have a thin (~1 nm) interfacial layer of SiO_2 that is formed during metal oxide deposition, which helps to reduce the interface-trap density in as-processed devices [42].

In this chapter, we report the total ionizing dose (TID) response of HfO_2-SiO_2/SiGe *p*MOS FinFETs under different irradiation biases. Negative bias irradiation leads to the worst-case degradation in the TID response of these devices. We attribute this to the additional contributions of radiation-induced holes generated in the SiO_2 interfacial layer of the bilayer insulating structure that, under negative bias, transport into and become trapped in the HfO_2. This leads to a more negative threshold voltage shift, compared to 0 V irradiation. During positive bias irradiation, a similar number of radiation-induced electrons are generated in the SiO_2. These can similarly transport into and become trapped in the HfO_2, leading to a less negative threshold voltage shift than during 0 V irradiation.

Experimental details

*p*MOS FinFETs were fabricated on SOI wafers with strained $Si_{0.75}Ge_{0.25}$ fins. After the SiGe fin etching process, an HfO_2 layer (~2 nm) was formed by atomic layer deposition, and TiN and amorphous-Si were deposited. A ~1 nm SiO_2 interfacial layer (IL) was formed between the HfO_2 and SiGe fin. Through this process, a high quality interface on SiGe can be achieved without the need for a Si cap layer [41]. The devices used in this study have a fin width (W_{fin}) of 50 nm, fin length (L_{fin}) of 250 nm and fin height (H_{fin}) of ~40 nm. This HfO_2/SiGe *p*MOS FinFET structure is shown schematically in Fig. 3.1(a). A TEM picture of the gate dielectric given in Fig. 3.1(b) clearly shows a SiO_2 interfacial layer existing between SiGe channel and HfO_2 dielectric.



(a) (b)

Fig. 3.1. (a) schematic and (b) TEM cross-section of a SiGe *p*MOS FinFET with HfO_2/SiO_2 gate dielectric.

Unlidded devices were irradiated at a dose rate of 31.5 krad(SiO_2)/min using a 10-keV ARACOR x-ray source, under positive, negative, and 0 V bias. I_D-V_G curves were measured to determine threshold voltage shifts (ΔV_{th}), and components due to oxide-trap charge (ΔV_{ot}) and

effective interface-trap (ΔV_{it}) density using the midgap charge separation technique [6] effective interface-trap (ΔV_{it}) density using the midgap charge separation technique [26]. We note that the effective interface-trap density may also include contributions from border traps [43]. Stress-induced degradation without irradiation was also measured at comparable irradiation times and biases. All irradiations and electrical stresses and measurements were performed at room temperature. At least three devices were measured for each case.

Experimental results and discussion

Fig. 3.2 shows the drain current I_D at V_{SD} = 50 mV and transconductance G_m versus gate voltage V_G as a function of total dose at room temperature. The devices were irradiated up to 2 Mrad(SiO_2) at a gate bias of −2 V, with all other terminals grounded. The I_D-V_G curves shift negatively with total dose, consistent with the buildup of net oxide-trap charge in the HfO_2 dielectric layer [38],[39],[44],[45]. A stretch-out of the I_D-V_G curves and a decrease in peak G_m are observed, consistent with the generation of interface traps.

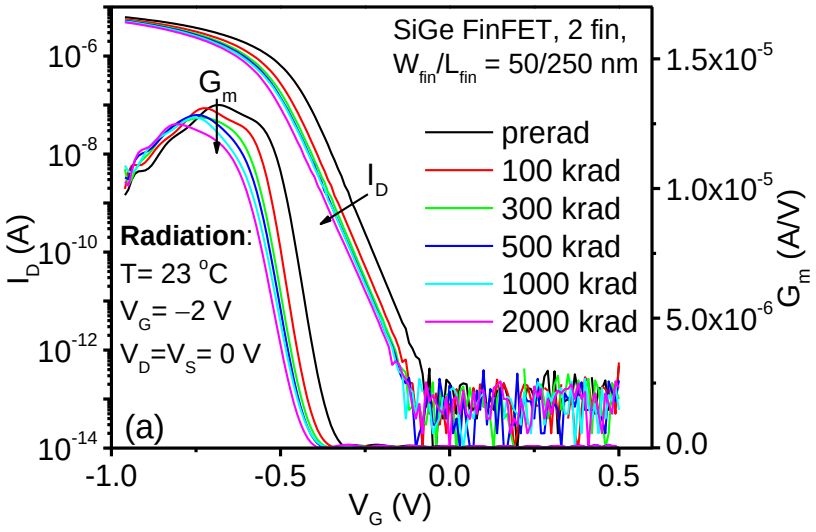


Fig. 3.2 Drain current I_D and transconductance G_m as a function of gate voltage V_G and varying total dose with applied gate bias of −2 V on devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm.

In Fig. 3.3, SiGe *p*MOS FinFETs are subjected to the same negative bias stress as in Fig. 3.2, with and without irradiation. In order to correct for the effect of the charge trapping that occurs as a result of electrical stress, adjusted values of purely radiation-induced ΔV_{th} (blue triangles) are obtained by subtracting ΔV_{th} due to negative bias stress without irradiation (black squares) from that due to negative-bias irradiation under negative bias (red circles). For these devices, irradiation appears to have a more significant effect on the device operating characteristics than negative bias stress.

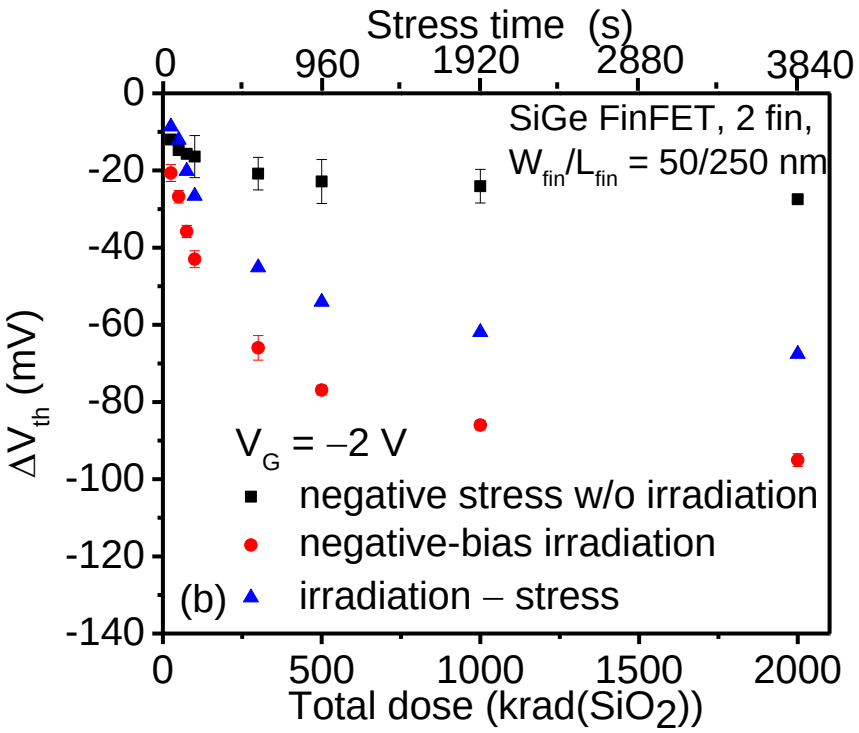


Fig. 3.3 Threshold voltage shift due to negative-bias irradiation as a function of total dose and due to negative stress without irradiation as stress time on devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm.

Fig. 3.4 shows the threshold voltage shifts as a function of total dose and corresponding stress times at an applied gate bias of +1.5 V for SiGe *p*MOS FinFETs with a HfO_2/SiO_2 gate dielectric stack. No significant threshold voltage shifts are observed for these devices under

similar stressing conditions for positive gate bias, without irradiation, indicating negligible stress-induced negative charge trapping in the bulk of the HfO_2/SiO_2. Thus, we conclude that the threshold voltage shifts observed during positive bias X-ray exposure are only induced by the irradiation.

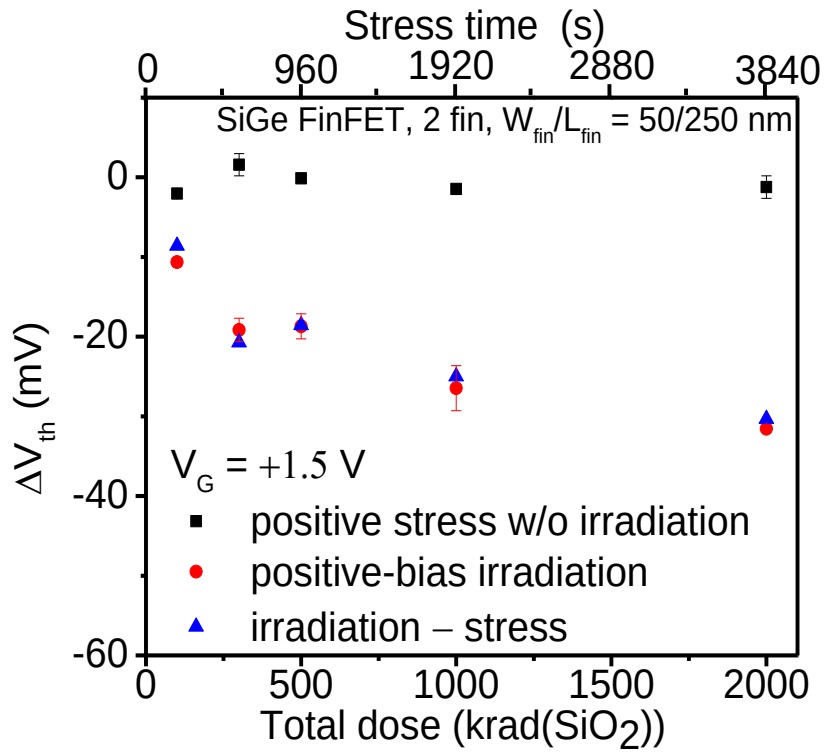


Fig. 3.4 ΔV_{th} as a function of dose for SiGe *p*MOS FinFETs irradiated with 10-keV X-rays at a dose rate of 31 krad(SiO_2)/min and as function of stress time without irradiation under +1.5 V.

Fig. 3.5 shows the adjusted radiation responses of SiGe *p*MOS FinFETs irradiated with 10-keV X-rays up to 2 Mrad(SiO_2). The applied biases are +1.5 V for positive-bias irradiation and −2 V for negative-bias irradiation to obtain a similar magnitude of electric field ($|E_{ox}| \approx 10$ MV/cm). The largest threshold shift is observed for negative-bias irradiation, in contrast to what is typically observed for Si devices with SiO_2 or HfO_2 gate dielectrics [44].

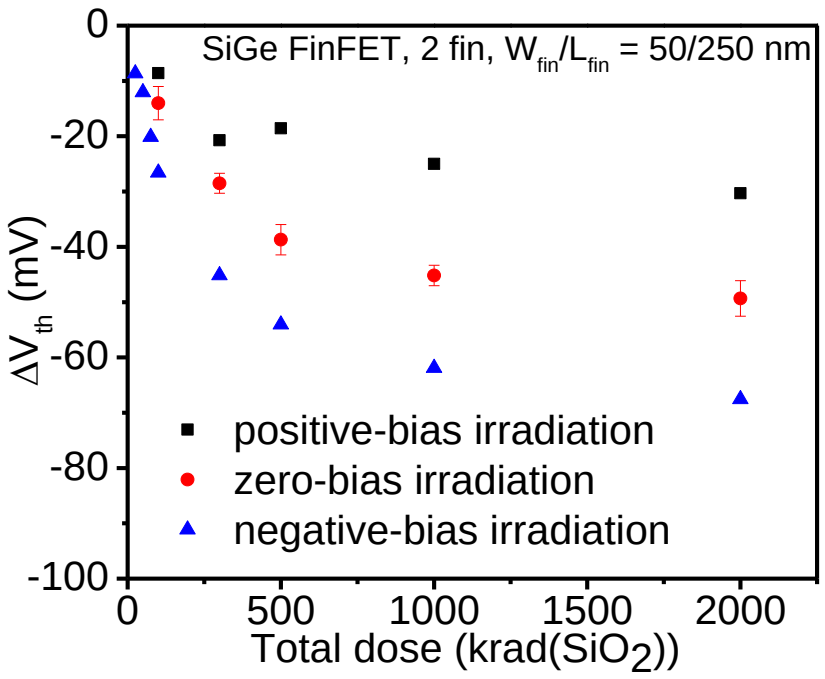
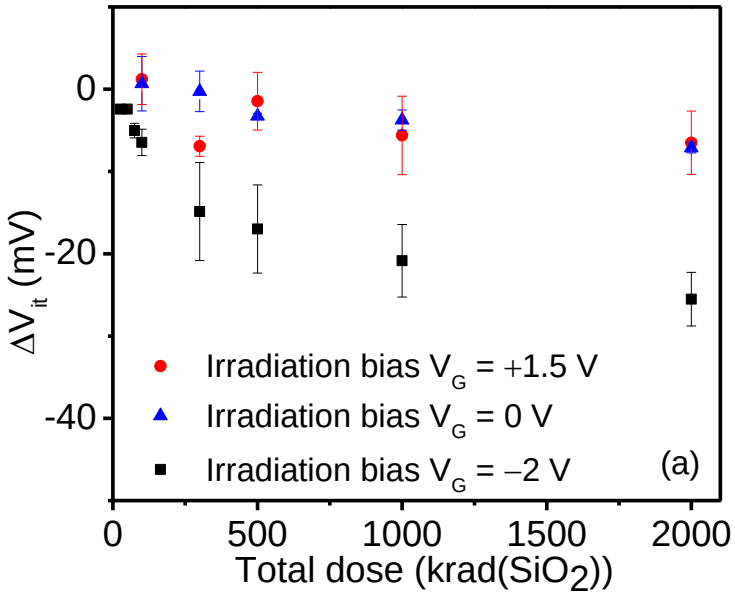
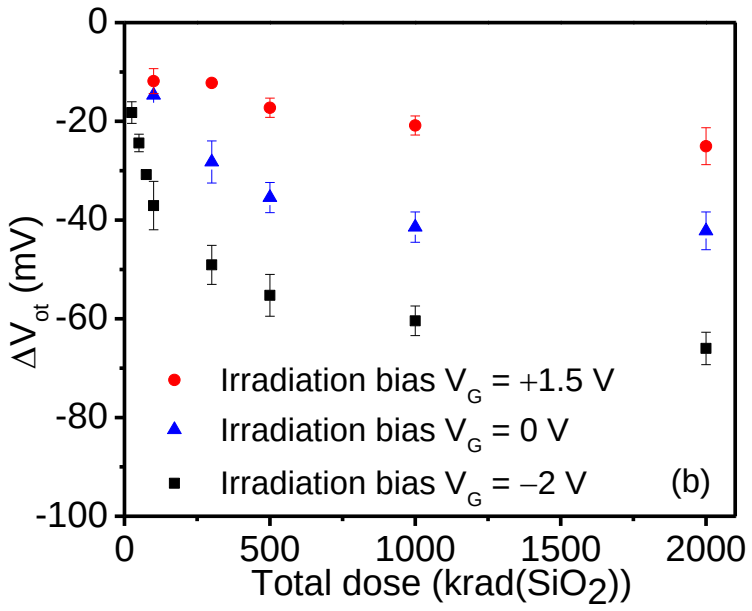


Fig. 3.5 Adjusted ΔV_{th} as a function of dose under different irradiation bias conditions. The gate biases during irradiation are +1.5 V, 0 V, and –2 V.



(a)



(b)

Fig. 3.6 (a) ΔV_{it} and (b) ΔV_{ot} as a function of total dose on devices of fin length/width (W_{fin}/L_{fin}) ratio = 50 nm/250 nm at room temperature. The gate biases applied during irradiation are +1.5 V, 0 V and −2 V.

In Fig. 3.6(a) and 5(b), ΔV_{it} and ΔV_{ot} are plotted for the devices of Fig. 3.5, respectively. The largest shifts for both ΔV_{it} and ΔV_{ot} are observed for negative-bias irradiation. HfO_2 is known to trap both electrons and holes efficiently during radiation exposure [45],[46]. The values of ΔV_{ot} for 0 V irradiation reflect net positive charge trapping in the HfO_2, demonstrating an excess of trapped holes relative to trapped electrons in this case.

The results of Figs. 3.5 and 3.6 are reminiscent of the responses of thicker bilayer Si_3N_4/SiO_2 structures [47]-[49] that similarly pair an overlying material (Si_3N_4) that traps both electrons and holes efficiently with a SiO_2 layer with much lower trap density. There the excess electron trapping observed during negative bias irradiation results from radiation-induced holes that are generated in the SiO_2 and transport into the Si_3N_4 and become trapped, leading to a more

negative threshold voltage shift than would be observed otherwise. Similarly, during positive bias irradiation, radiation-induced electrons generated in the SiO_2 can transport into the Si_3N_4 and become trapped, leading to a more positive threshold voltage shift. To see if these HfO_2 structures may respond in a similar fashion, we estimate the percentage of radiation-induced electrons and holes $f_{e,h}$ generated in the SiO_2 that would have to be trapped in the HfO_2 in Figs. 4 and 5 to account for the differences in response with radiation bias using the expression [50]:

$$f_{e,h} = \frac{\pm \Delta V_{e,h} \varepsilon_{ox}}{q \kappa_g f_y t_{ox}^2 D} \tag{1}$$

Here $\Delta V_{e,h}$ is the difference in threshold voltage shift due to excess electron or hole trapping as a result of the mechanism described above, ε_{ox} is the dielectric constant of SiO_2, $-q$ is the electronic charge, κ_g is the number of electron-hole pairs generated per unit dose in SiO_2 (~8.1×10^{12} $cm^{-3}rad^{-1}(SiO_2)$), f_y is the charge yield of SiO_2, t_{ox} is the physical thickness of SiO_2 (~1 nm), and D is the total dose. We obtain first-order estimates of the values of $\Delta V_{e,h}$ by comparing the values of ΔV_{ot} at positive, negative, and 0 V bias in Fig. 5. Specifically, $\Delta V_e \approx (\Delta V_{ot})_{+1.5V\ bias} - (\Delta V_{ot})_{0V\ bias}$ and $\Delta V_h \approx (\Delta V_{ot})_{-2V\ bias} - (\Delta V_{ot})_{0V\ bias}$. The charge yield f_y is estimated as 0.9 from [13 or Fig. 2.2]. The dose enhancement factor is estimated to be 2.5 for a thin SiO_2 layer surrounded by TiN, HfO_2, and Si from [51]. Applying these assumptions to the 2 Mrad(SiO_2) data in Fig. 5(b), we estimate an effective value of 14% for f_h and 10% for f_e. These results are quite plausible for [52]. However, previous work in Si FinFETs with SiO_2 gate dielectric show that contributions of trapped charges in the buried oxide [53] may contribute to the differences in radiation response observed in Figs. 3.5. Fig. 3.7 shows that the lateral gates provide good electrostatic control of the potential both in the BOX and in the fin in narrow-fin device. FinFETs used in this work are approximately 20 nm narrower than the drawn fin width (e.g., 50 nm fin drawn width is really 30 nm fin device width actual). So the influence of the

lateral gates is strong in the 50 nm fin drawn width to prevent hole trapping in the BOX. Moreover, the stretchout of I_D-V_G in Fig. 3.2 is negligible, which is very different from that in Si/SiO_2 FinFETs in [53]. Therefore, the BOX likely has a weak influence on the radiation response in this work.

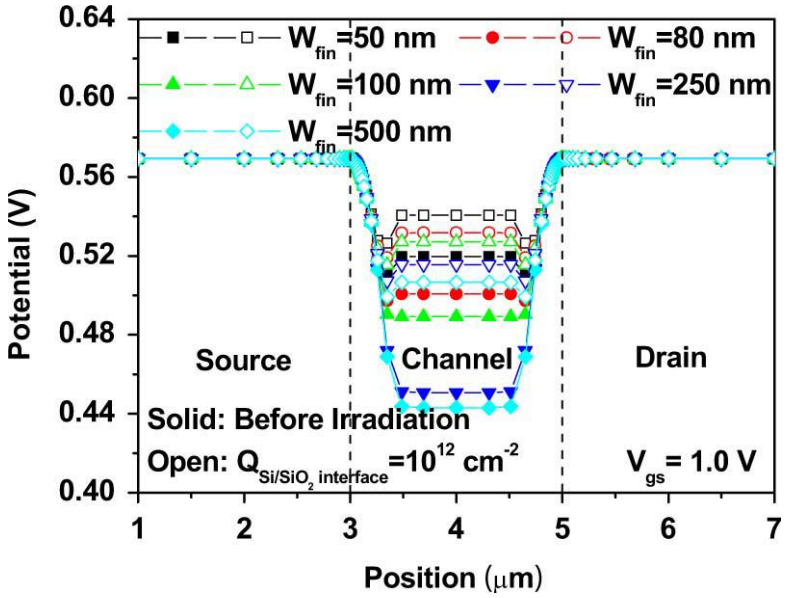


Fig 3.7 Simulated distribution of the electrostatic potential in the silicon, at fin/BOX interface, along the source/drain axis. The gate bias is 1.0 V. After [53].

The effective interface-trap buildup in these devices is smaller than the trapped-positive charge buildup, and is maximized for negative-bias irradiation. This suggests that the interface (or border) traps in these devices are not created via the release of hydrogen in the HfO_2 or SiO_2 layer, but may instead be due to hydrogen that is released from dopant atoms in the SiGe channel layer [54].

Summary of Chapter, and Conclusions

In this chapter, we report the irradiation and bias stress responses of SiGe *p*MOS FinFETs with HfO_2/SiO_2 gate dielectric stacks irradiated with 10-keV x-rays up to 2 Mrad(SiO_2).

Experimental results suggest that negative bias irradiation leads to the worst-case degradation in the total dose response of SiGe *p*MOS FinFETs. We attribute this result to an increase in density of radiation-induced holes that are generated in the SiO_2 interfacial layer and trapped in the HfO_2 under negative bias, as compared with the 0 V irradiation case, as compared to the case of positive bias, when additional electron trapping occurs in the HfO_2 layer.

CHAPTER IV

NEGATIVE BIAS TEMPERATURE INSTABILTY IN SILICON GERMANIUM *p*MOSFETS

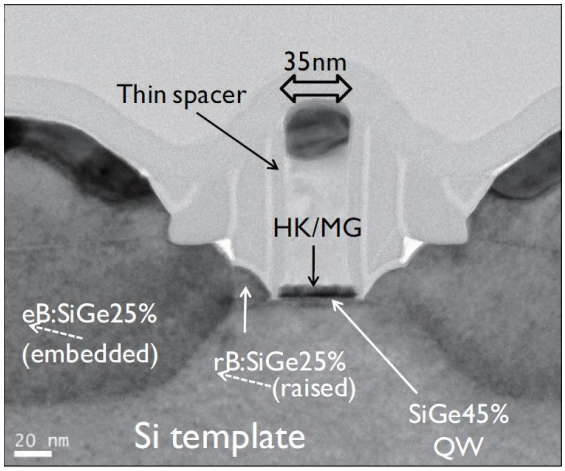
Temperature and negative-bias stress-induced degradation in SiGe *p*MOSFETs with Si cap layer and SiO_2/HfO2/TiN gate stacks is reported. Due to its enhanced hole mobility, strained SiGe is a promising alternative channel candidate material to boost *p*MOSFET performance for sub-22 nm technologies [55]. By using a thin Si cap layer for SiGe surface passivation, control of the SiGe/high-k interface has been successfully achieved [56].

In this chapter, interface- and oxide-trap charge buildup during negative bias-temperature stress of $SiGe_{0.45}$ *p*MOSFETs is investigated. We compare the activation energies (E_a) of the effective interface trap and oxide trap charge densities in $SiGe_{0.45}$ *p*MOSFETs with SiO_2/HfO_2 gate dielectric stacks with those in Si FinFETs with SiO_2 gate dielectrics. We find similar values of E_a for oxide-trap charge buildup for the two device types, and a reduced E_a for interface-trap buildup for the $SiGe_{0.45}$ *p*MOSFETs with high-k gate stacks, compared to the Si FinFETs with SiO_2 gate dielectrics.

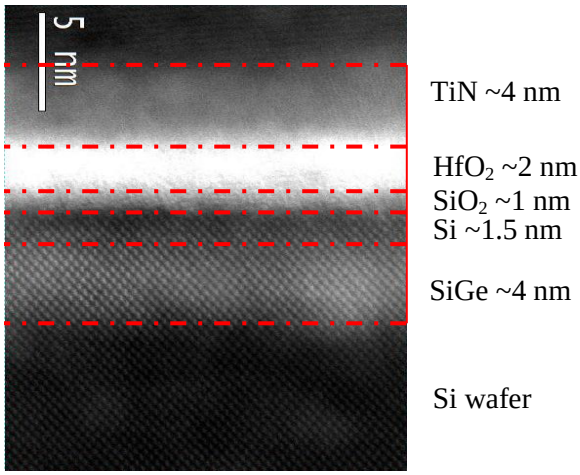
Experimental Details

The buried SiGe channel *p*MOSFETs used in this chapter were fabricated at the Interuniversity Microelectronics Centre (imec). A TEM picture of the device structure is depicted in Fig. 4.1(a). The $SiGe_{0.45}$ *p*MOSFETs were fabricated on an *n*-type Si wafer with a 4.0 nm $SiGe_{0.45}$ layer deposited onto a 2.0 nm Si buffer. A 1.4 nm Si cap was partially oxidized, yielding an unconsumed 1.0 nm thick Si cap layer to passivate the $SiGe_{0.45}$ surface and improve

the interface quality [see Fig. 4.1(b)]. On top of the SiO_2 interfacial layer (IL), a ~1.5 nm HfO_2 layer and TiN metal gate was deposited by atomic layer deposition (ALD) and physical vapor deposition (PVD), respectively [57]. The equivalent oxide thickness (EOT) of the gate dielectric stack is 1.5 nm. Due to the valence-band offset between SiGe and the Si cap (band diagram is shown in Fig 4.3), inversion holes are confined in the SiGe channel, which therefore acts as an implant free quantum well (IFQW).



(a)



(b)

Fig. 4.1 (a) TEM and (b) high resolution STEM cross-section of a SiGe *p*MOSFET with HfO_2/SiO_2 gate dielectric.

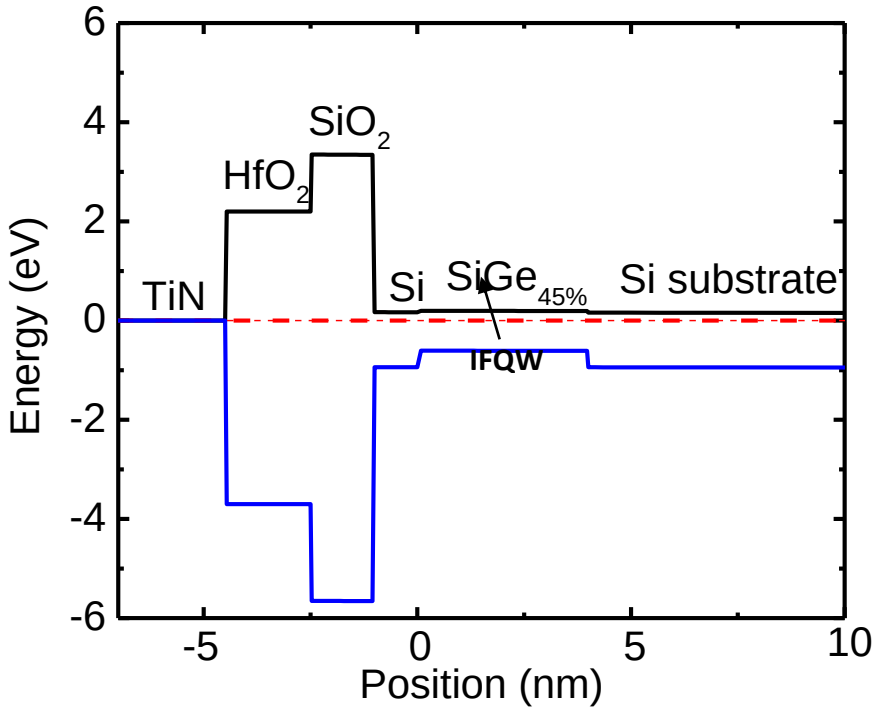


Fig. 4.2 Band diagram sketch of SiGe device.

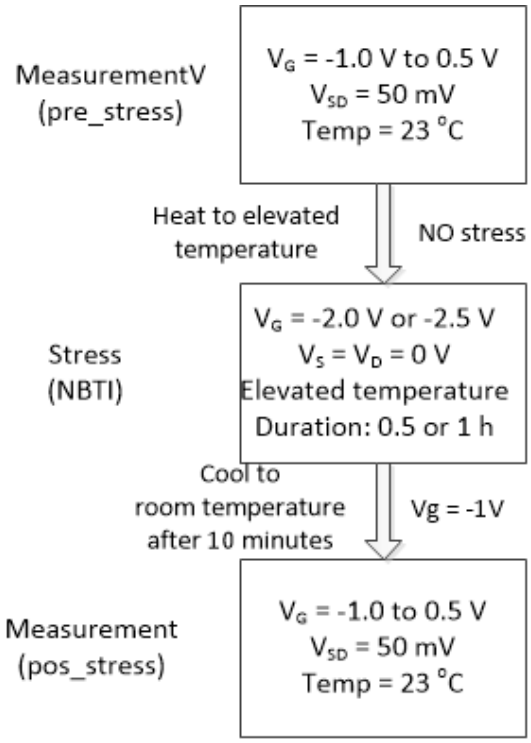
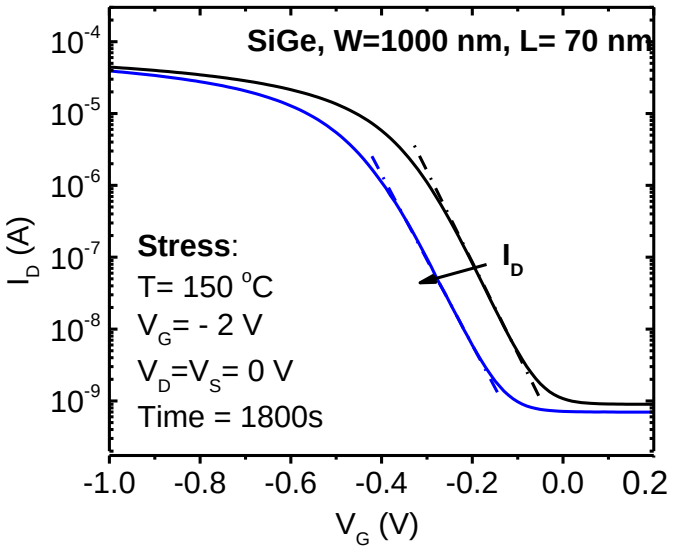


Fig. 4.3 NBTI experiment measurement flow chart.

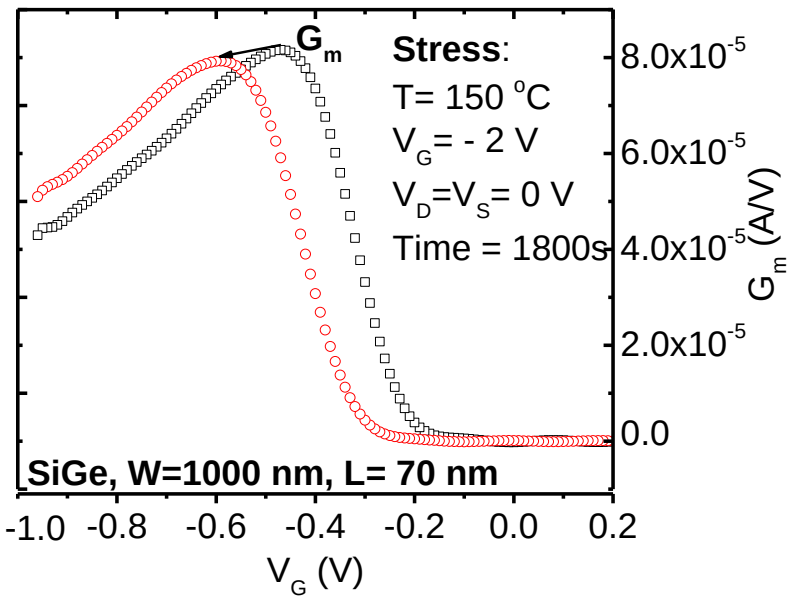
NBTI stress experiments were performed using the measure–stress–measure technique, as shown in Fig. 4.3. The SiGe *p*MOSFETs were heated with a hot chuck and held at a constant temperature under negative bias. The holding temperatures vary from 125 ℃ to 250 ℃. The post-stress I_D-V_G curves were taken after the samples cooled to room temperature. For comparison of the charge trapping properties, Si *p*MOSFETs with 2 nm SiO_2 gate dielectrics [58] were also measured. $SiGe_{0.45}$ and Si devices were stressed at −2.5 V (−11.1 MV/cm) and −2 V (−10.3 MV/cm), respectively.

Experimental Results and Analysis

Fig. 4.4 shows the I_D-V_G and transconductance G_m characteristics as a function of gate voltage V_G measured at room temperature before and after negative gate bias stress at −2 V. The I_D-V_G curves shift negatively after 30 min of negative gate bias, which means that positively charged defects are generated during NBTI stress. The peak G_m is reduced with bias-temperature stress, which is due to the reduction of carrier mobility in the channel caused by charges trapped at (interface traps), or very close to (border traps), the Si/SiO_2 interface.



(a)

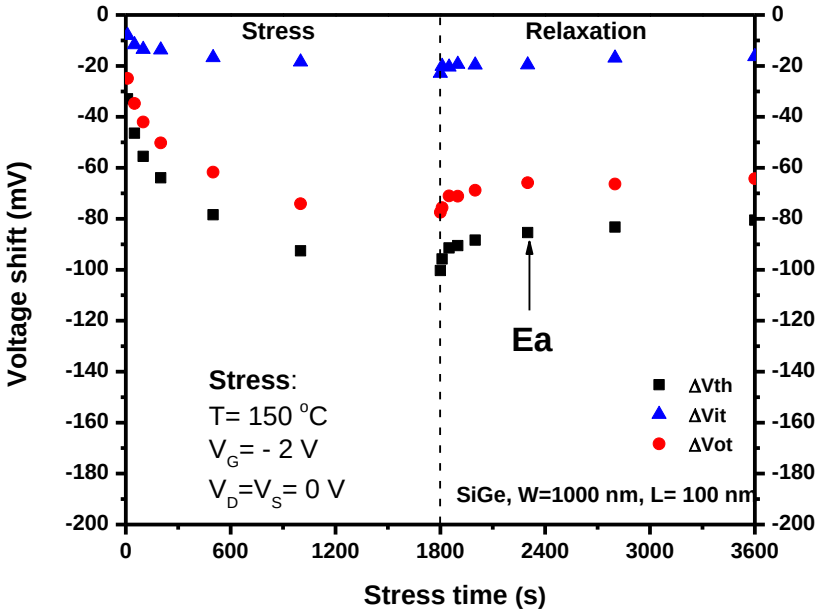


(b)

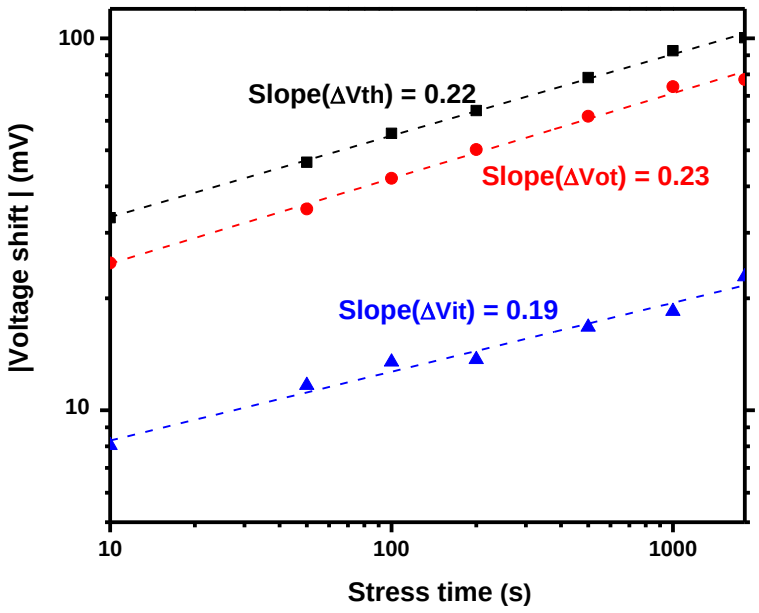
Fig 4.4 (a) I_D-V_G and (b) G_m characterization as a function of gate voltage V_G measured at room temperature for a 1 μm × 0.07 μm $SiGe_{0.45}$ *p*MOSFET after 30 min stress time. The stress bias is −2 V on the gate and the stress temperature is 150 ℃.

The atomic-scale defect observed by ESR shows that NBTI is likely due to two components: hole trapping in pre-existing bulk oxygen vacancies (ΔN_{ot}) and interface traps associated with the creation of new defects at the Si/SiO_2 interface (ΔN_{it}). Threshold voltages due to oxide-trap ΔV_{ot} and effective interface-trap charge ΔV_{it} are estimated via the subthreshold swing separation method introduced in Chapter 2, and shown as a function of stress and recovery time in Fig. 4.5(a). The threshold voltage shift is mainly due to oxide-trap charge, with a smaller contribution from interface traps. And about 25% of the degradation is recovered for the 1800 s recovery time. The activation energies of ΔN_{ot} and ΔN_{it} have been determined after the fastest annealing traps are emptied. Fig. 4.5(b) shows that V_{th} and its components due to oxide and interface trap charge have power law time dependences; the ~0.21 ± 0.02 time exponents are

similar to values observed for ΔV_{th} in previous work for $Si/SiO_2/HfO_2/TiN$ structures [59], suggesting the same hole trapping and interface bond-breaking process.

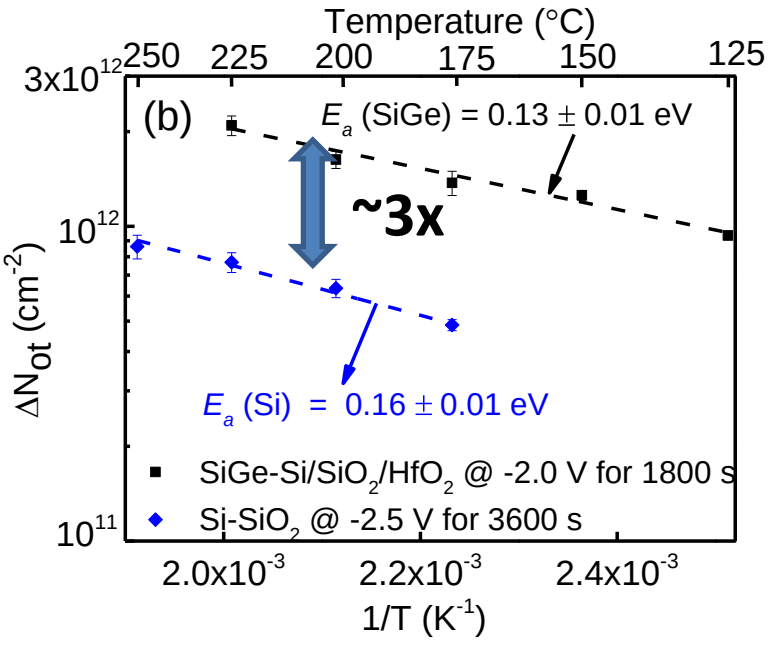


(a)

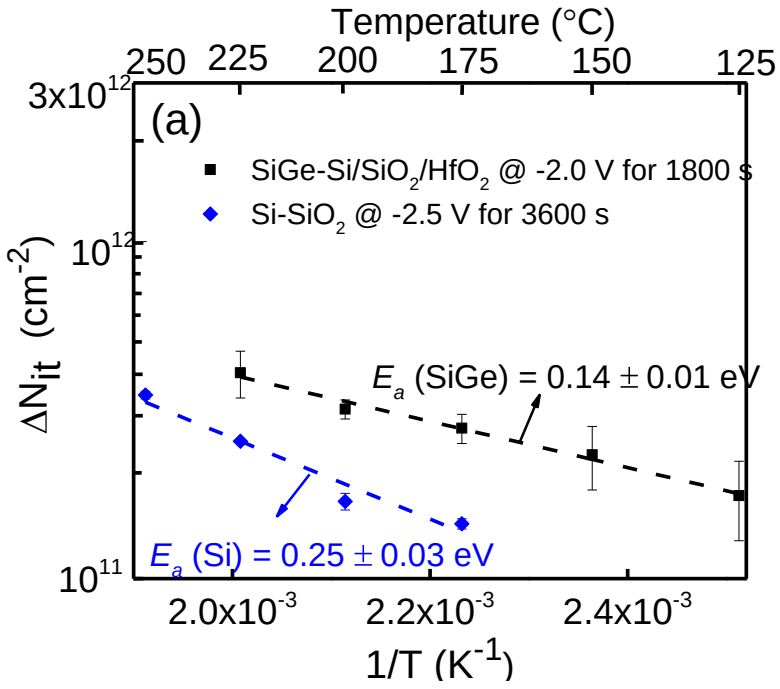


(b)

Fig. 4.5 (a) Overall threshold voltage shift ΔV_{th}, as well as components due to oxide trap charge ΔV_{ot} and interface traps ΔV_{it}, as a function of stress time for $SiGe_{0.45}$ *p*MOSFETs with W/L = 1 μm/0.1 μm at 150 ℃ for V_{stress} = −2 V and $V_{relaxation}$ = 0 V. (b) shows stress time exponents for ΔV_{th}, ΔV_{ot} and ΔV_{it}.



(a)



(b)

Fig. 4.6 Arrhenius plots of (a) interface trap generation ΔN_{it} and (b) oxide trap charge ΔN_{ot} for $SiGe_{0.45}$ *p*MOSFETs with high-k dielectrics stressed for 30 min at −11.1 MV/cm and for Si *p*MOSFETs with SiO_2 dielectric stressed for 60 min at −10.3 MV/cm.

Arrhenius plots are shown in Fig. 4.6. The activation energy values for interface trap generation $E_{a,it}$ for $SiGe_{0.45}$ and Si *p*MOSFETs are 0.14 ± 0.01 eV and 0.25 ± 0.03 eV, respectively. The $E_{a,it}$ values for Si are similar to those reported in the literature [28],[60]. The value of E_a for the interface trap buildup in the $SiGe_{0.45}$ structures is significantly reduced as compared with the Si/SiO_2 structure. In contrast, the extracted activation energy for oxide trap charge $E_{a,ot}$ is 0.16 ±0.01 eV for $SiGe_{0.45}$ *p*MOSFETs with high-k gate stacks and 0.13 ±0.01 eV for Si pMOSFETs with SiO_2 gate dielectrics, as shown in Fig. 3(b) [60]. Moreover, the SiGe device with SiO_2/HfO_2 gate stacks shows both higher oxide traps (~3x) and interface traps than the Si device with SiO_2 dielectric. J. Franco et al. reported that incorporation of Ge into the channel can significantly reduce NBTI degradation [61], as shown in Fig. 4.7. In the work of Franco et al., both the Si and SiGe devices have a SiO_2/HfO_2 gate dielectric stack. The contradiction is ascribed to higher trap densities in SiGe/ SiO_2/HfO_2 gate stack than Si/SiO_2 gate dielectric.

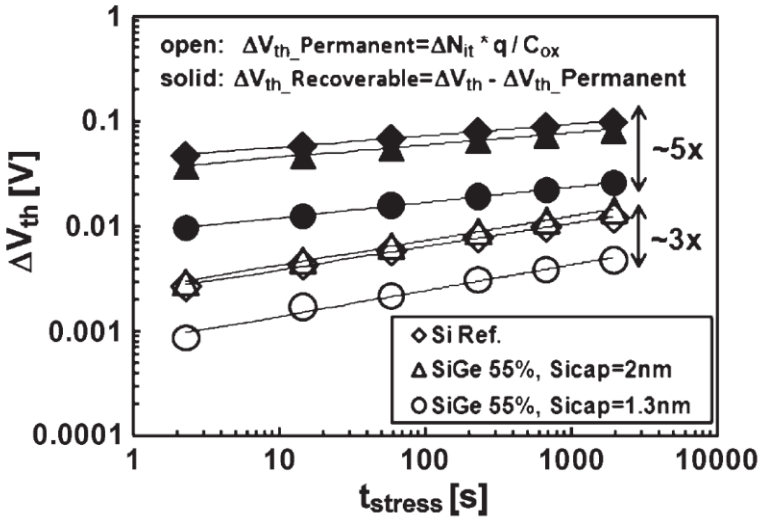


Fig. 4.7 Total ΔV_{th} split into the so-called permanent (P) ΔV_{th}, assumed to be caused by ΔN_{it}, and the recoverable (R) ΔV_{th}, assumed to be caused by filling of pre-existing oxide traps (N_{ot}). SiGe devices with a thinner Si cap show both reduced P and R.

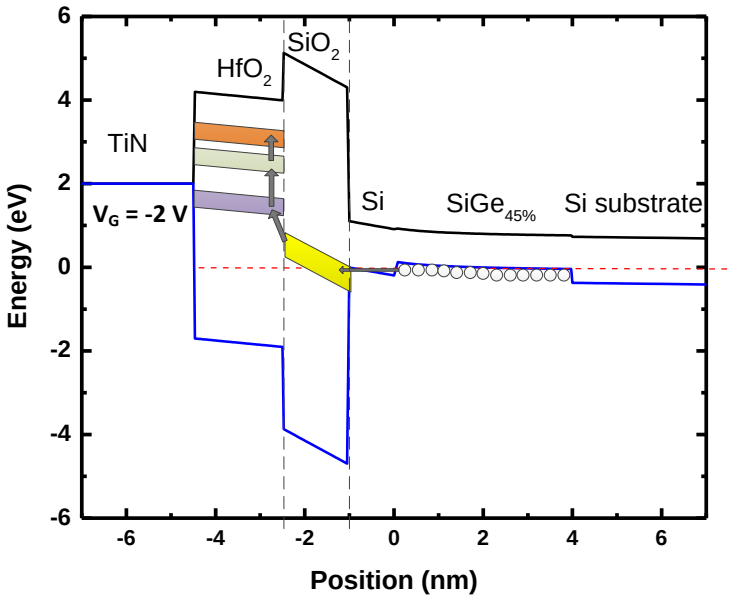


Fig. 4.8 Schematic diagram for negative gate bias in SiGe *p*MOSFETs including different defect bands associated with oxygen vacancies in the interfacial layer and HfO_2.

Oxide-trap charges

Fig. 4.8 shows the band diagram for negative gate bias, including pre-existing bulk oxide vacancy energy levels in interfacial SiO_2 and HfO_2. Similar activation energies for oxide-trap charge indicate both cases likely are dominated by hole tunneling into oxygen vacancies in near-interfacial SiO_2 and HfO_2. Holes from the SiGe channel first tunnel into oxygen vacancies in interfacial SiO_2, and then are trapped in deep defects in HfO_2. This may explain why most oxide trapped charges are stable after the 1800s recovery time shown in Fig. 4.5(a).

Interface traps

The SiGe layer thicknesses (~4 nm) are well below the critical relaxation thickness for the used epitaxial processes, causing the SiGe channel layer to be strained [62]. Therefore, the lattice of Si cap matches that of underlying Si substrate. The lattice match between Si cap and

substrate can also be discriminated from high resolution STEM picture in Fig. 4.1 (b). Strain effects at the Si/SiO_2 interface were not involved in this SiGe device.

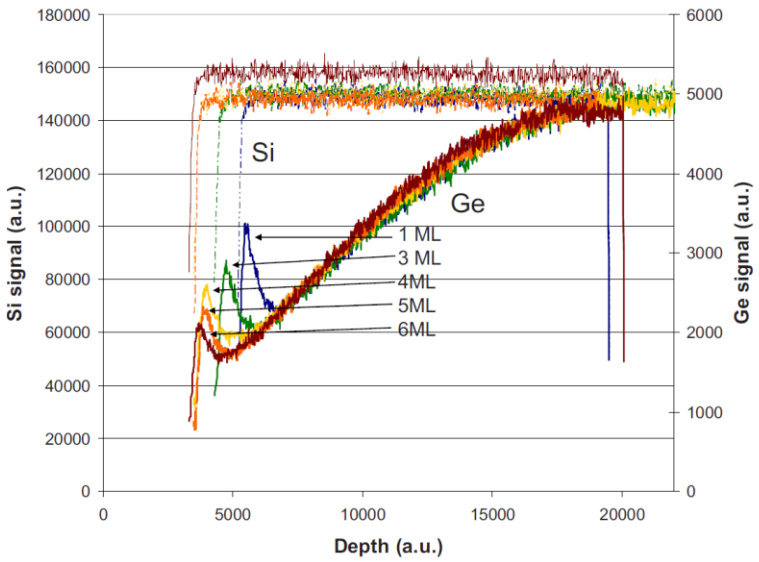


Fig. 4.9 Ge and Si depth profiles in Si layers with increasing thickness on SiGe. After [63].

Previous work reported by M. Caymax et al. [63] found that surface segregation of Ge through the Si cap layer takes place during the cap layer growth. Figure 4.9 shows Ge and Si depth profiles in Si cap layer during the growth of cap layer. A certain amount of Ge extends into the Si cap layer from the SiGe channel with a small Ge peak at the surface. Density functional cluster calculations by E. S. Tok et al. [64] show that germanium dimers exert little influence on the hydrogen desorption barriers of neighboring silicon or germanium dimers. However, a relatively larger effect upon desorption barrier is observed when germanium atoms are present in the second layer below top silicon layer. This suggests that interface-trap creation processes, which are due to breaking Si-H bond, involving germanium present near Si-H (at the same layer or below) need lower energy than those at a pure SiO_2/Si interface, leading to a lower activation energy of interface traps.

Summary of Chapter and Conclusions

We have found that I_D-V_G curves shift negatively due to hole trapping, and G_m is reduced due to interface-trap charge buildup during temperature-bias stress in SiGe *p*MOSFETs. The threshold voltage shift is mainly due to oxide-trap charge, with a smaller contribution from interface traps. NBTI induced oxide trapped charges and interface trap densities were determined at different temperatures, and then activation energies were extracted from Arrhenius plots. Our experimental results show similar values of E_a for oxide-trap charge buildup, and a reduced E_a for interface-trap buildup in *p*MOSFETs with $Si_{0.55}Ge_{0.45}$ channel and high-k gate stacks, compared to Si channel devices with SiO_2. Similar activation energies for oxide-trap charges are primarily due to hole trapping in O vacancies. While activation energies for interface traps in SiGe *p*MOSFETs are likely affected by Ge atoms around Si-H in the Si cap layer that overlies the SiGe channel.

CHAPTER V

SUMMARY AND CONCLUSION

This thesis investigates the radiation response (TID) and reliability (NBTI) of SiGe devices with high-k dielectric layers. The 10-keV x-ray irradiation and bias stress response of SiGe *p*MOS FinFETs with HfO_2/SiO_2 gate dielectric stacks up to 2 Mrad(SiO_2) has been evaluated. Experimental results suggest that negative bias irradiation leads to the worst-case degradation in the total dose response of SiGe *p*MOS FinFETs. We attribute this result to the additional contributions of radiation-induced holes generated in the SiO_2 interfacial layer of the bilayer insulating structure that, under negative bias, transport into and become trapped in the HfO_2, as compared with the 0 V irradiation case. HfO_2 has also been shown to trap large amounts of radiation-induced electrons. During positive bias irradiation, a similar number of radiation-induced electrons are generated in the SiO_2 and become trapped in HfO_2, leading to a less negative threshold voltage shift than during 0 V irradiation.

Negative bias-temperature stress of $SiGe_{0.45}$ *p*MOSFETs is also investigated. We have found that I_D-V_G curves shift negatively due to hole trapping, and G_m is reduced due to interface-trap charge buildup during temperature-bias stress in SiGe *p*MOSFETs. The threshold voltage shift is mainly due to oxide-trap charge, with a smaller contribution from interface traps. NBTI induced oxide trapped charge and interface trap densities were determined at different temperatures; then activation energies were extracted from Arrhenius plots. Our experimental results show similar values of E_a for oxide-trap charge buildup, and a reduced E_a for interface-trap buildup in *p*MOSFETs with $Si_{0.55}Ge_{0.45}$ channel and high-k gate stacks, compared to Si

channel devices with SiO_2. The similar activation energies for oxide-trap charge are primarily due to hole trapping in O vacancies. The activation energy for interface traps in SiGe *p*MOSFETs likely affected by Ge atoms around Si-H in the Si cap layer that overlies the SiGe channel. A certain Ge is observed to extend into the Si cap layer from the SiGe channel with a small Ge peak at the surface. The density functional cluster calculations suggest that the Ge atoms near the surface can decrease the hydrogen desorption barriers of neighboring silicon.

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